In the Specification:

Please replace paragraph 56 with the following amended paragraph:

The adjustable delay element 116 is programmed as follows. As seen in Fig. 4, the adjustable delay element 116 is comprised of flip-flop 1000, flip-flop 1002 and multiplexer 1004. The desired delay is implemented by first, setting the PDDLY to one. This sets the multiplexer 1004 to select the output of flip-flop 110. Otherwise, flip-flops 1000 and 1002 are not placed in the circuit and no delay is implemented. When PDDLY is set to one, the data path signal will necessarily pass through the two flip-flops 1000 and 1002. These flip-flops 1000 and 1002 have inherent delay. Moreover, the amount of delay is implemented by varying the frequency of the FAST clock. Thus, the delay becomes one cycle of the FAST clock, plus a small amount of delay caused by flip-flops 1000 and 1002.